Faculty of Engineering
Benha university
Electrical Eng.Dept.
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Design of Electronic Circuits(E401)
Final-Term Exam
Date: 28/5/2016
Time: 3 Hours

Answer all the following questions:

Q1: Design a BJT differential amplifier that provides two single-ended outputs. The amplifier is to have a differential gain of at least 100 V/V , a differential input resistance $\geq 10\ k\Omega$, and a common mode gain no greater than 0.1 V/V. Use a 2-mA current source for biasing. Give the complete circuit with component values and suitable power supplies that allow for ± 2 V swing at each collector. The BJTs available have $\beta \geq 100$.

Q2:The 4-stages direct coupled op-amp circuit shown in Fig.(1) is operating at room temperature. Assuming all transistors have $\beta = 200$.

a) Perform an approximate dc analysis to calculate the current and voltage everywhere in the circuit (assuming $|V_{BE}|=0.7v$, neglect the Early effect). Note that Q_6 has four times the area of each of Q_9 and Q_3.

b) Compute the differential input resistant.

c) Compute the overall voltage gain of the multistage amplifier.
What is the input offset voltage if R_1 changed by 2%

Q3: For the current mirror shown in Fig.(2), derive an expression for the current transfer function $I_o(s)/I_i(s)$ as a function of transistor parameters taking into account the BJT internal capacitances and neglecting r_x and r_o . Assume the BJTs to be identical.

Q4: Consider the complementary BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat}. For ±10V power supplies and a 100Ω load resistance,

a) What is the maximum sine wave output power available?
b) What is the power-conversion efficiency?
c) Show how to reduce the zero-crossing distortion in class B power amplifier?

Q5: The circuit shown in Fig.(3) consists of a differential stage followed by an emitter follower, with series–shunt feedback supplied by the resistors R_1 and R_2. Assuming that the dc component of V_s is zero, and that β of the BJTs is very high, find:

a) The dc operating current of each of the three transistors and show that the dc voltage at the output is approximately zero.
b) The open loop gain (A).
c) The feedback gain (B).
d) The input resistance R_{in}, and The output resistance R_{out}. Assume that the transistors have $\beta = 100$.

PTO

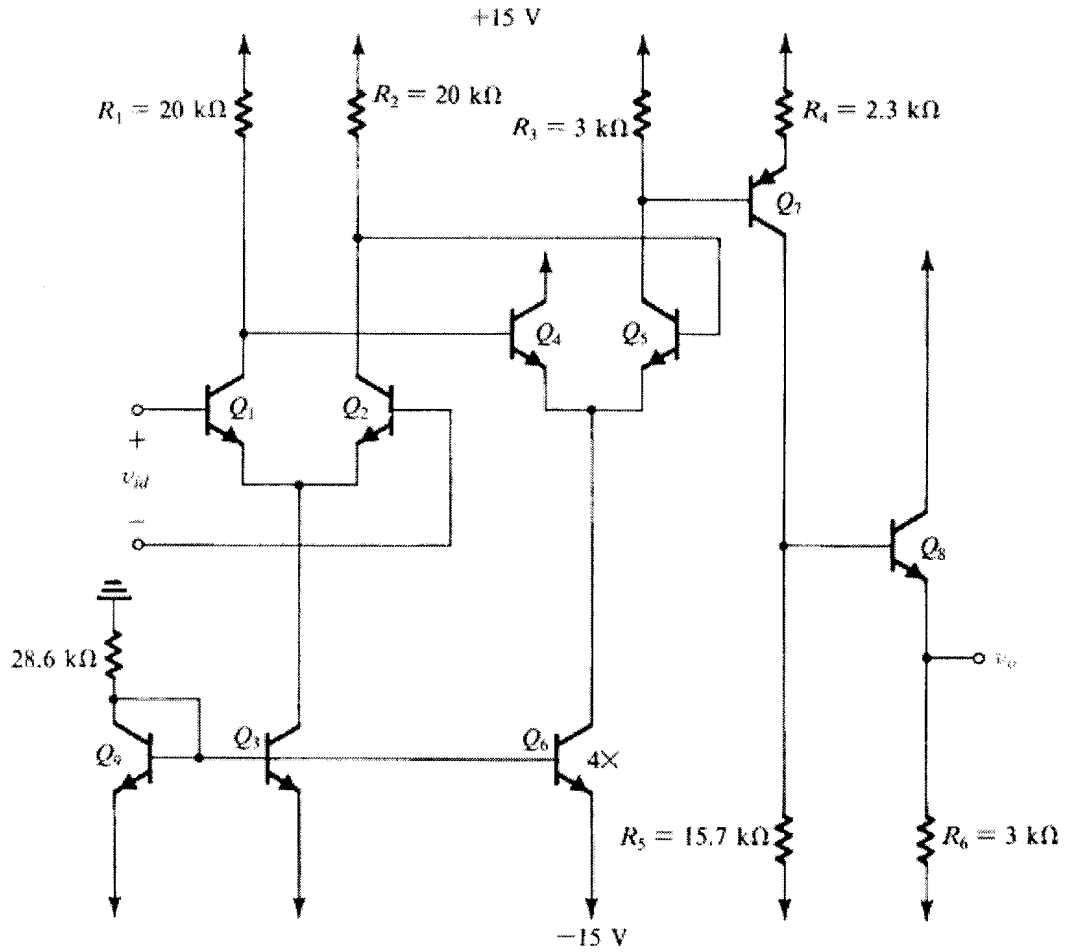


Fig. (1)

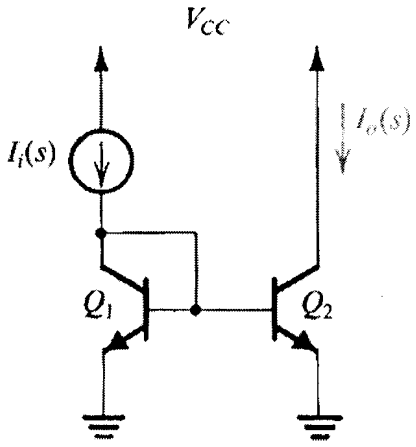


Fig. (2)

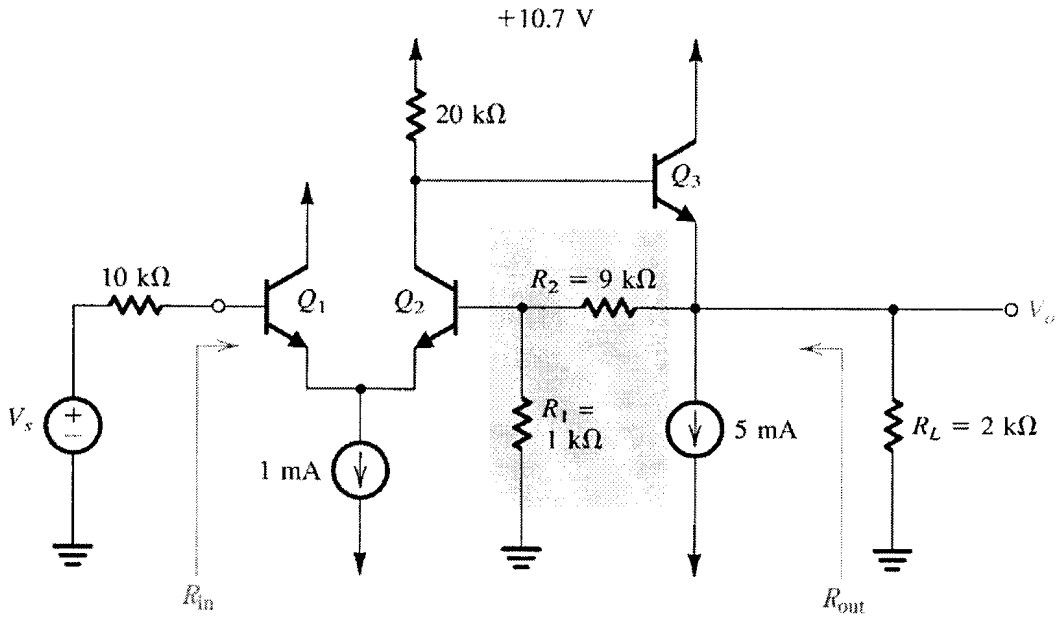


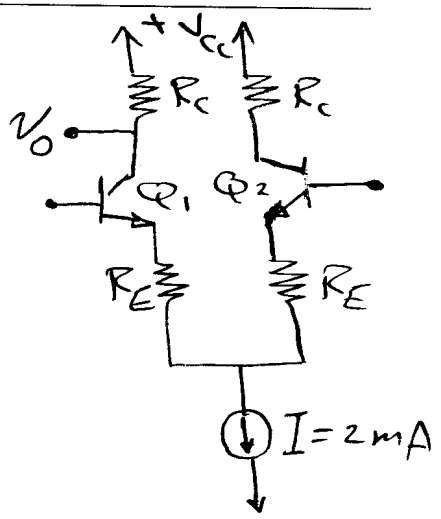
Fig. (3)

BEST WISHES

Hossam Labib

Q1: Design a BJT differential amplifier that provides two single-ended outputs. The amplifier is to have a differential gain of at least 100 V/V , a differential input resistance ≥ 10 kΩ, and a common mode gain no greater than 0.1 V/V. Use a 2- mA current source for biasing. Give the complete circuit with component values and suitable power supplies that allow for ± 2 V swing at each collector. The BJTs available have $\beta \geq 100$.

Solution:



From DC

$\therefore 2I_E = I \Rightarrow I_E = \frac{I}{2}$

$\therefore I_E = 1mA$

$r_e = \frac{V_T}{I_E} = \frac{25mV}{1mA} = 25\Omega$

$\because R_{id} \geq 10\ K\Omega \Rightarrow$ Let $R_{id} = 10K\Omega$

$\because \beta \geq 100 \Rightarrow \beta = 100$

for $r_e = 25\Omega \Rightarrow$ There is must be R_E in the differential Amplifier To met the design requirement of $R_{id} \geq 10K\Omega$.

$\therefore R_{id} = 2(1+\beta)(r_e + R_E)$

$10K = 2(1+100)(25 + R_E)$

$R_E = \frac{10K}{2*101} - 25 = 25\Omega$

- For differential gain $A_d = 100\ V/V$ and Two single ended O/P $\Rightarrow A_d = \frac{V_o}{V_{id}} = \frac{V_{c1}}{V_{id}} = \frac{\text{Total resistance at Collector}}{\text{Total resistance at emitter}}$

$A_d|_{\text{single ended}} = \frac{R_c}{2r_e + 2R_E} = \frac{R_c}{2(r_e + R_E)} = 100$

$100 = \frac{R_c}{2(25+25)} \Rightarrow R_c = 10K\Omega$

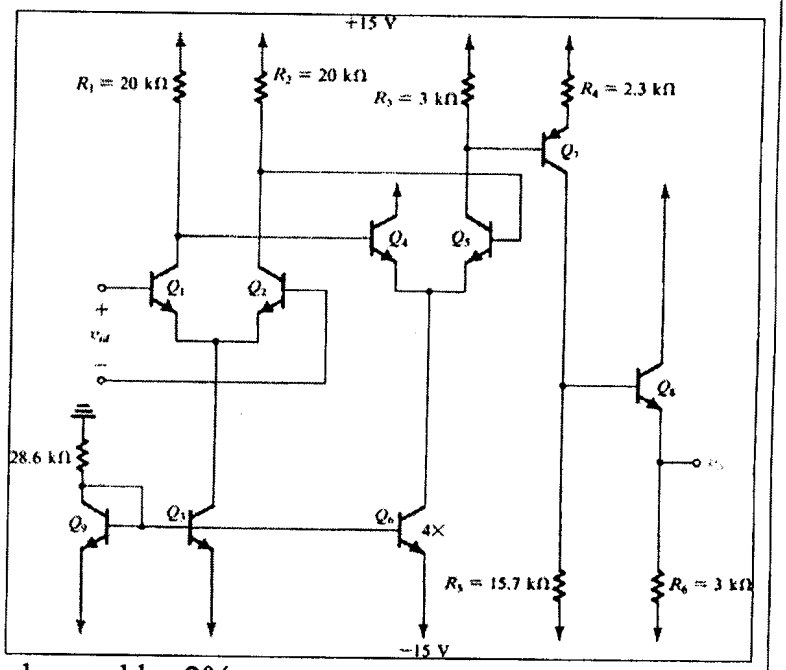
- For $\pm 2V$ swing $\Rightarrow V_{c1} = V_{c2} = 2V = V_c$

$\because V_c = V_{cc} - I_c R_c \Rightarrow V_{cc} = V_c + I_c R_c = 2 + 1M \times 10K$

$V_{cc} = 12\ V$ ' Then $V_{cc} = \pm 12V$

Q2:

The 4-stages direct coupled op-amp circuit shown in Fig.1 is operating at room temperature. Assuming all transistors have $\beta = 200$



a) Perform an approximate dc analysis to calculate the current and voltage everywhere in the circuit (assuming $|V_{BE}|$=0.7v, neglect the Early effect). Note that Q_6 has four times the area of each of Q_9 and Q_3.

b) Compute the differential input resistant.

c) Compute the overall voltage gain of the multistage amplifier.

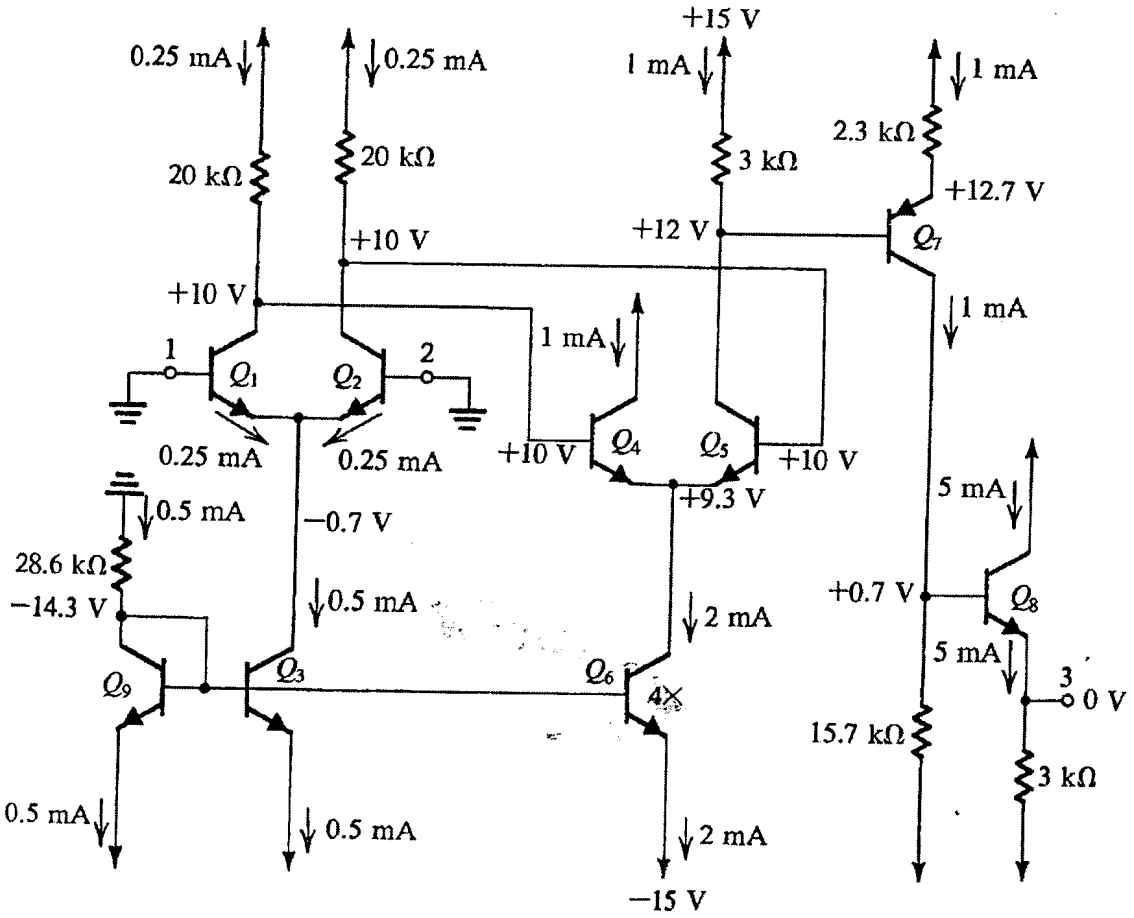
d) What is the input offset voltage if R_1 changed by 2%

Solution:

(a) The values of all dc currents and voltages are indicated on the circuit diagram. These values were calculated by ignoring the base current of every transistor-that is, by assuming β to be very high. The analysis starts by determining the current through the diode-connected transistor Q_9 to be 0.5 mA. Then we see that transistor Q_3 conducts 0.5 mA and transistor Q_6 conducts 2mA. The current-source transistor Q_3 feeds the differential pair (Q_1, Q_2) with 0.5 mA. Thus each of Q_1 and Q_2 will be biased at 0.25 mA. The collectors of Q_1 and Q_2 will be at [+15 - 0.25 x 20] =+10 V.

Proceeding to the second differential stage formed by Q_4 and Q_5, we find the voltage at their emitters to be [+10 - 0.7] = 9.3 V. This differential pair is biased by the current-source transistor Q_6, which supplies a current of 2 mA; thus Q_4 andQ_5 will each be biased at 1 mA. We can now calculate the voltage at the collector of Q_5 as [+15 - 1 x 3] = +12 V. This will cause the voltage at the emitter of the pnp transistor Q_7 to be + 12. 7 V, and the emitter current of Q_7 will be (+15 -12.7)/2.3 = 1 mA. The collector current of Q_7, 1 mA, causes the voltage at the collector to be [-15 + 1 x 15.7] = +0.7 V. The emitter of Q_8 will be 0.7 V below the base; thus output terminal 3 will be at 0 V.

Finally, the emitter current of Q8 can be calculated to be [0 - (-15)]/3 = 5 mA.



(b)The input differential resistance R_{id} is given by:

$$Rid = r_{\pi 1} + r_{\pi 2}$$

Since Q_1 and Q_2 are each operating at an emitter current of 0.25 mA, it follows that

$$r_{e1}=r_{e2}= 25/0.25=100\Omega$$

for $\beta = 200$; then

$$r_{\pi 1}= r_{\pi 2} = 201 \times 100 = 20.1\ k\Omega$$

Thus $R_{id} = 40.2k\Omega$

(c)To evaluate the gain of the first stage we first find the input resistance of the second stage, R_{i2},

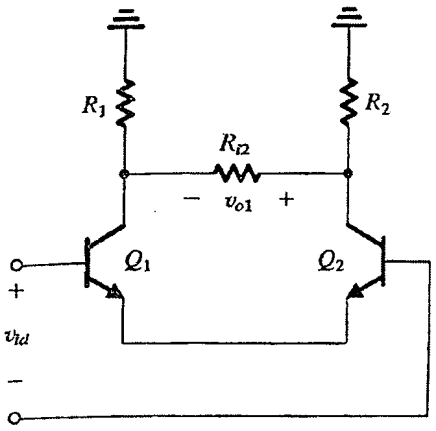
$$R_{i2} = r_{\pi 4}+ r_{\pi 5}$$

Q_4 and Q_5 are each operating at an emitter current of 1mA; thus

$$r_{e4} = r_{e5} = 25\ \Omega$$

$$r_{\pi 4}= r_{\pi 5}= 201 \times 25 = 5.025\ k\Omega$$

Thus $R_{i2} = 10.05\ k\Omega$.



This resistance appears between the collectors of Ql and Q2, as shown in - Fig. Thus the gain of the first stage will be

$$A1 \equiv \frac{v_{o1}}{v_{id}} \cong \frac{\text{Total resistance in collector circuit}}{\text{Total resistance in emitter circuit}} = \frac{R_{i2} \parallel (R_1 + R_2)}{r_{e1} + r_{e2}}$$

$$= \frac{10.05k \parallel 40k}{200} = \frac{8031.97}{200} = 40.16 \ {}^{V}/_{V}$$

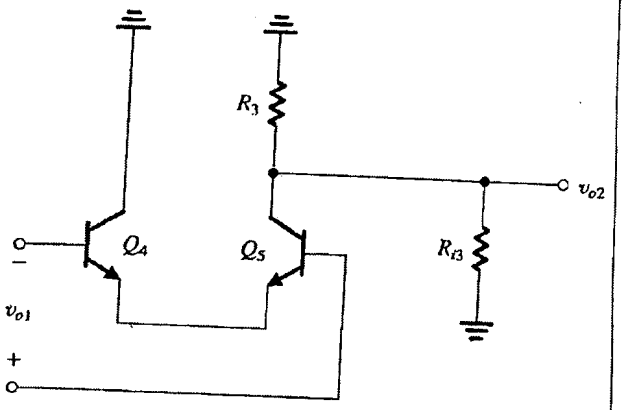


Figure 2 shows an equivalent circuit for calculating the gain of the second stage. As indicated, the input voltage to the second stage is the input voltage of the first stage, v_{o1}. Also shown is the resistance R_{i3} which is the input resistance of the third stage formed by Q_7 .The value of R_{i3} can be found by multiplying the total resistance in the emitter of Q_7 by (β+ 1):

$$R_{i3} = (\beta + 1)(R4 + re7)$$

Since Q_7 is operating at an emitter current of 1 mA,

$$r_{c7} = 25/1 = 25\Omega$$

$$R_{i3} = 201 \text{ x } (2.3k+25) = 467.325 \text{ k}\Omega$$

We can now find the gain A2 of the second stage as the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit:

$$A2 = \frac{v_{o2}}{v_{o1}} = -\frac{(R_3 \parallel R_{i3})}{r_{e4} + r_{e5}}$$

$$= -\frac{(3k \parallel 467.325k)}{50} = \frac{2980.86}{50} = -59.6 \ {}^{V}/_{V}$$

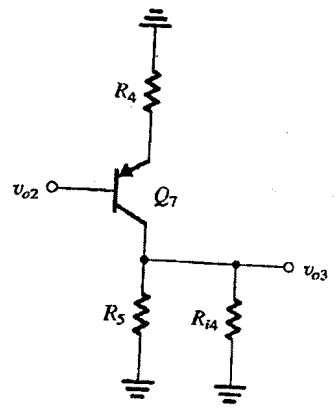
To obtain the gain of the third stage we refer to the equivalent circuit shown in Fig., where R_{i4} is the input resistance of the output stage formed by Q8. Using reflection resistance-reflection rule, we calculate the value of R_{i4} as

$$R_{i4} = (\beta + 1)(r_{e8} + R_6)$$

where

$$r_{e8} = 25/5 = 5\Omega$$

$$R_{i4} = 201(5 + 3000) = 604.005 \text{ k}\Omega$$

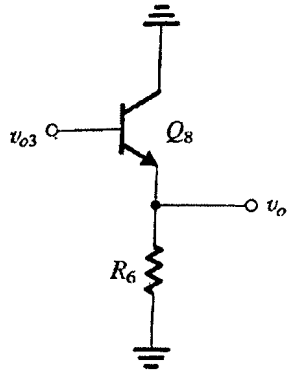


The gain of the third stage is given by

$$A3 \equiv \frac{v_{o3}}{v_{o2}} = -\frac{(R_5 \parallel R_{i4})}{r_{e7} + R_4} = -\frac{(15.7k \parallel 604.005k)}{25 + 2.3k}$$
$$= -\frac{15.302k}{2.325k} = -6.58\ {}^{V}/_{V}$$

Finally, to obtain the gain A4 of the output stage we refer to the equivalent circuit in Fig. and write

$$A4 \equiv \frac{v_o}{v_{o3}} = \frac{R_6}{R_6 + r_{e8}} = \frac{3000}{3000 + 5} = 0.998 \simeq 1$$



The overall voltage gain of the amplifier can then be obtained as follows:

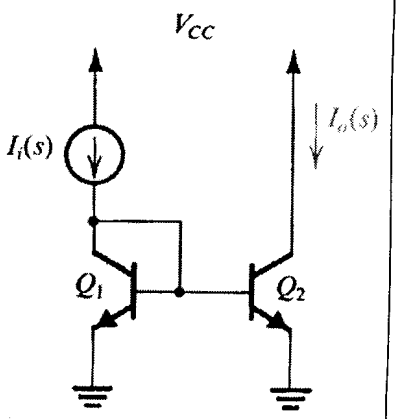
$$\frac{v_o}{v_{id}} = A1A2A3A4 = 40.16 \times -59.6 \times -6.58 \times 1 = 15749.5$$

(d) The input offset voltage if R_1 changed by 2%

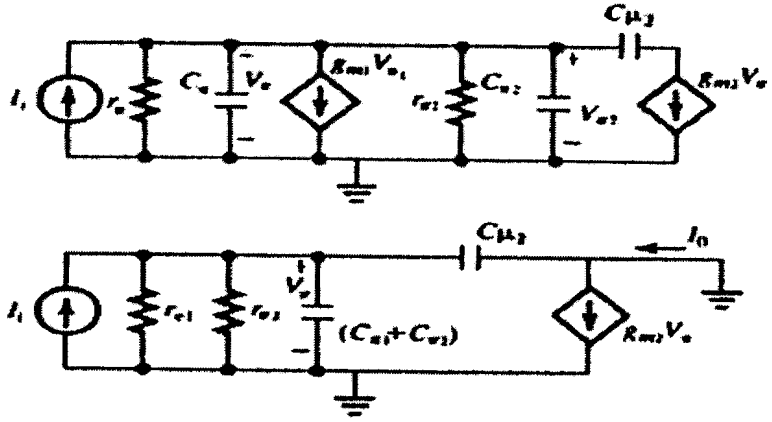
The input offset voltage V_{OS}

$$|V_{OS}| = V_T\left(\frac{\Delta R_c}{R_c}\right) = V_T\left(\frac{\Delta R_1}{R_1}\right) = 25m \times 0.02 = 0.5mV$$

Q3:For the current mirror shown in Fig.(2), derive an expression for the current transfer function $I_o(s)/I_i(s)$ as a function of transistor parameters taking into account the BJT internal capacitances and neglecting r_x and r_o. Assume the BJTs to be identical.



Solution:



$$V_\pi = \frac{I_i}{\left(\frac{1}{r_{e1}} + \frac{1}{r_{\pi 2}}\right) + s(C_{\pi 1} + C_{\pi 2} + C_{\mu 2})}$$

$$I_o = g_{m2}V_\pi - C_\mu s V_\pi$$

$$= \frac{(g_{m2} - C_\mu s)I_i}{\left(\frac{1}{r_{e1}} + \frac{1}{r_{\pi 2}}\right) + s(C_{\pi 1} + C_{\pi 2} + C_{\mu 2})}$$

$$\frac{I_o}{I_i} = \frac{g_{m2} - C_\mu s}{\left(\frac{1}{r_{e1}} + \frac{1}{r_{\pi 2}}\right) + s(C_{\pi 1} + C_{\pi 2} + C_{\mu 2})}$$

$$I_{C1} = I_{C2} \Rightarrow r_{\pi 1} = r_{\pi 2},$$

$$g_{m1} = g_{m2},\ C_{\pi 1} = C_{\pi 2}$$

$$\frac{I_O}{I_i} = \frac{g_m - C_\mu s}{\left(\frac{1}{r_e} + \frac{1}{r_\pi}\right) + (C_\mu + 2C_\pi)s}$$

$$= \frac{1 - \frac{C_\mu}{g_m}s}{\left(\frac{1}{g_m r_e} + \frac{1}{g_m r_\pi}\right) + s\frac{C_\mu + 2C_\pi}{g_m}}$$

$$g_m r_e = \frac{I_C}{V_T}\frac{V_T}{I_E} = \alpha = \frac{\beta}{\beta + 1}$$

$$g_m r_\pi = \beta$$

$$\Rightarrow \frac{I_O}{I_i} = \frac{1 - \frac{C_\mu}{g_m}s}{1 + \frac{1}{\beta} + \frac{1}{\beta} + s(2C_\pi + C_\mu)/g_m}$$

$$\frac{I_o}{I_i} = \frac{1}{1 + \frac{2}{\beta}} \quad \frac{1 - s\frac{C_\mu}{g_m}}{1 + s\frac{(2C_\pi + C_\mu)}{g_m\left(1 + \frac{2}{\beta}\right)}}$$

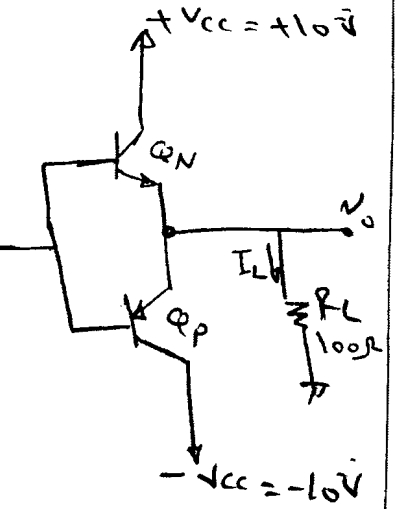
Q4:

Consider the complementary BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat}. For ±10V power supplies and a 100Ω load resistance,

a) What is the maximum sine wave output power available?

b) What is the power-conversion efficiency?

c) Show how to reduce the zero-crossing distortion in class B power amplifier?



Solution

(a) The average load power $P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$

where $\hat{V}_o$ is the peak amplitude of o/p sine-wave

- The maximum sine-wave o/p power occurs when $\hat{V}_o = V_{cc}$ Then

$$P_L|_{max} = \frac{1}{2}\frac{V_{cc}^2}{R_L} = \frac{1}{2}\frac{(10)^2}{100} = 0.5\ W$$

(b) The power conversion efficiency $\eta = \frac{P_L}{P_S}$

where P_S is the total supply power

$$P_S = P_{S+} + P_{S-}$$

∵ The average power drawn from each of the two power supplies will be the same - Then

$$P_{S+} = P_{S-} = \frac{1}{\pi}\frac{\hat{V}_o}{R_L}V_{cc} = \frac{1}{\pi}\frac{(10)}{100}*10 = 0.318\ W$$

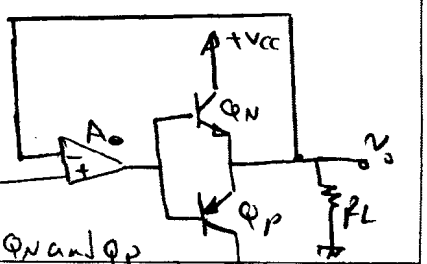
∴ $P_S = 2*0.318 = 0.637\ W$

∴ The power conversion efficiency η is

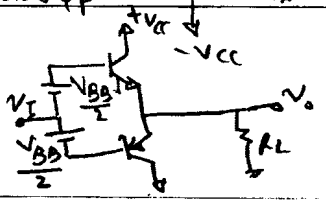
$$\eta = \frac{P_L}{P_S}*100 = \frac{0.5}{0.637}*100 = 78.5\ \%$$

(c) - To reduce the zero-crossing distortion in class B power Amp. by using a high-gain op-Amp. and overall negative feedback as shown The ±0.7V dead band is reduced to ±0.7/A_o volt.

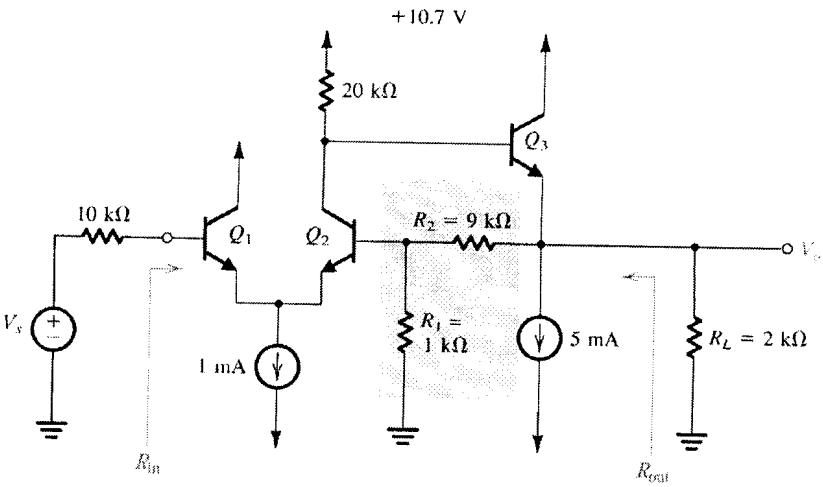
where A_o is the dc gain of op-Amp.



- OR by biasing the complementary transistors using bias voltage V_{BB} applied between the bases of Q_N and Q_p giving rise to a bias current I_Q. Thus for small v_I, both transistors conduct and crossover distortion is almost completely eliminated. as shown in fig. (class AB o/p stage)



Q5: The circuit shown in Fig.( ) consists of a differential stage followed by an emitter follower, with series–shunt feedback supplied by the resistors R_1 and R_2. Assuming that the dc component of V_s is zero, and that β of the BJTs is very high, find:



a) The dc operating current of each of the three transistors and show that the dc voltage at the output is approximately zero.

b) The open loop gain (A).

c) The feedback gain (B).

d) The input resistance R_{in}, and The output resistance R_{out}. Assume that the transistors have β = 100.

Solution:

$$I_{E1} = I_{E2} = 0.5\text{mA}$$

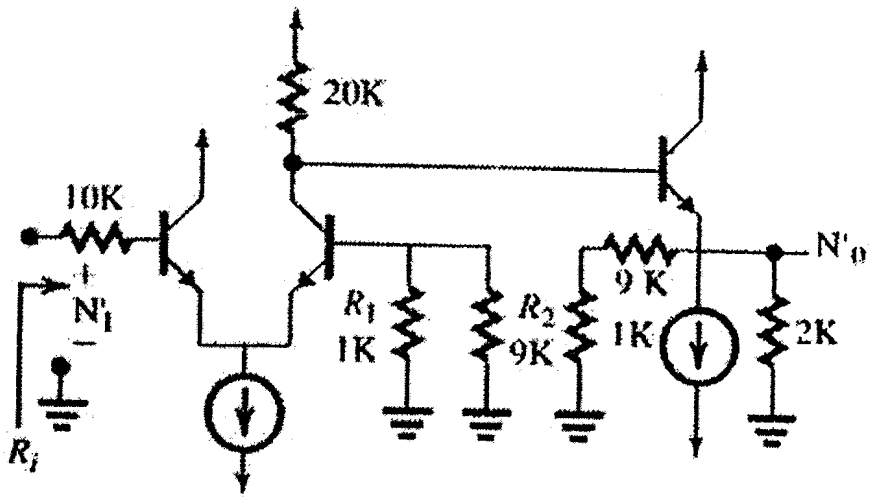
$$V_{C2} = 10.7 - 0.5 \times 20 = +0.7\text{v}$$

$$V_o = 0.7 - V_{BE3} = 0$$

$$I_{E3} = 5\text{ mA}$$

$$r_{e1} = r_{e2} = V_A / I = 50\Omega,\ r_{e3} = 5\Omega$$

A-Circuit:



$$A = \frac{V_o}{V_i} = \frac{[20 \parallel (\beta_2 + 1)(r_{e3} + 2 \parallel 10)]}{r_{e1} + r_{e2} + \frac{10}{\beta_1 + 1} + \frac{(1 \parallel 9)}{\beta_2 + 1}} \times$$

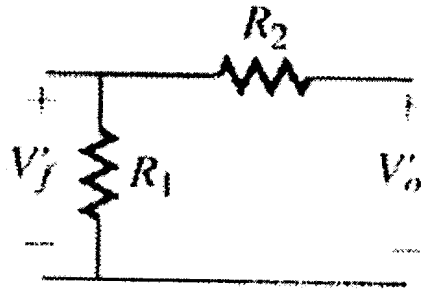
$$\frac{(2 \parallel 10)}{r_{e3} + (2 \parallel 10)} = 85.7 \text{ V / V}$$

$$R_i = R_S + (\beta + 1)(r_{e1} + r_{e2}) + R_E \parallel R_4$$

$$= 10 + 101(50 + 50) + (1 \parallel 9) = 21 \text{ k}\Omega$$

$$R_0 = 2 \parallel 10 \parallel \left[r_{e3} + \frac{20}{\beta_2 + 1} \right] = 181 \ \Omega$$

B-Circuit:



$$\beta = V_f' / V_o'$$

$$= \frac{1}{9 + 1} = 0.1 \text{ V / V}$$

$$A_f = \frac{V_o}{V_S} = \frac{A}{1 + A\beta} = \frac{85.7}{1 + 85.7 \times 0.1} = 8.96 \text{ V / V}$$

$$R_{if} = R_i(1 + A\beta) = 21 \times 9.57 = 201 \text{ k}\Omega$$

$$R_{iN} = R_{if} - R_S = 201 - 10 = 191 \text{ k}\Omega$$

$$R_{of} = (R_{out} \parallel R_L) = \frac{R_o}{1 + A\beta} = \frac{181}{9.57} = 18.8 \ \Omega$$

$$\Rightarrow R_{out} = 19.1 \ \Omega$$