Benha Faculty of Engineering | **Electrical Engineering Department**
4th Year Electronics | **Final Exam: 17 June 2014**
Examiner: Dr. Hatem ZAKARIA | **Time allowed: 3 Hours**

Large Scale Integrated Systems (E402)

Model Answer

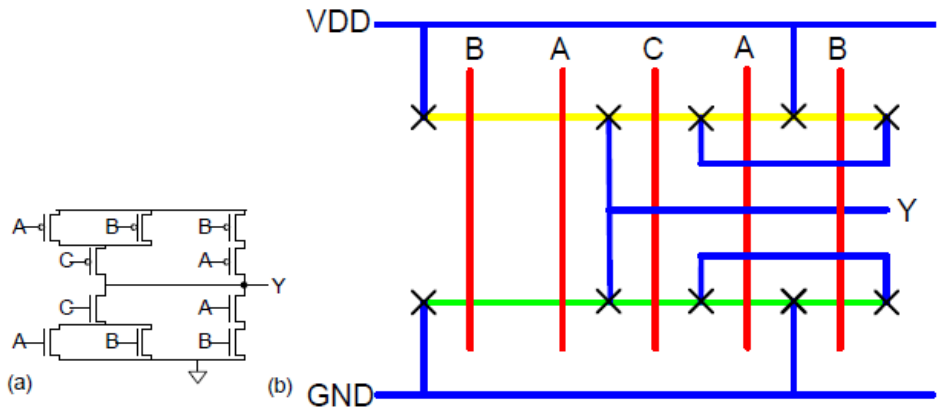
Question (1) **(25 Marks)**

a. State if the following statements are (✓) or (×) and justify your answer *'Note: Negation is not the answer'*:

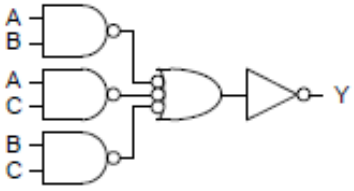
1. Scaling down of the transistor dimensions ***decreases*** the packaging density and increases the switching speed of the MOS circuits. (×)
2. Low power consumption of ***bipolar transistor*** allows for their very high integration density compared to ***MOS transistors***. (×)
3. For n-MOS circuits it is preferable to keep the substrate doping as ***high*** as possible. (×)
4. CMOS transmission gates are superior to n-MOS pass transistors because they can output strong ones and strong zeroes. (✓)
5. Polysilicon is better than metal for self-aligned gates. (✓)
   - It doesn't melt during later processing
6. For a 0.6 μm CMOS process, the parameter λ is equal to ***0.4 μm***. (×)
   - λ is equal to 0.3 μm
7. The minimum area of the n-MOS transistor channel $2\lambda \times 2\lambda$. (×)
   - $4\lambda \times 2\lambda$
8. The channel length modulation factor λ accounts for the increase of the drain current with V_{GS} in the saturation region. (×)
   - V_{DS}
9. The threshold voltage of a n-MOS transistor can be raised by applying ***a positive*** body voltage. (×)
10. In designing n-MOS pass transistor logic, it is preferable to drive a pass transistor with the output of another pass transistor. (×)
    - nMOS pass transistors pull no higher than V_{DD}-V_{tn}

b.

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



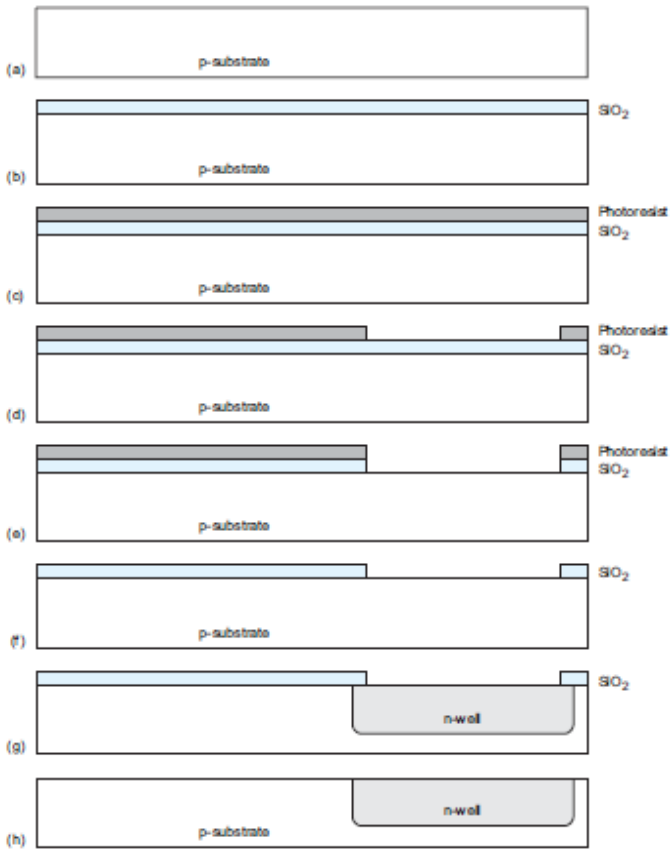
(c) 6 tracks wide x 7 tracks high = (48 x 56) = 2688 λ^2.



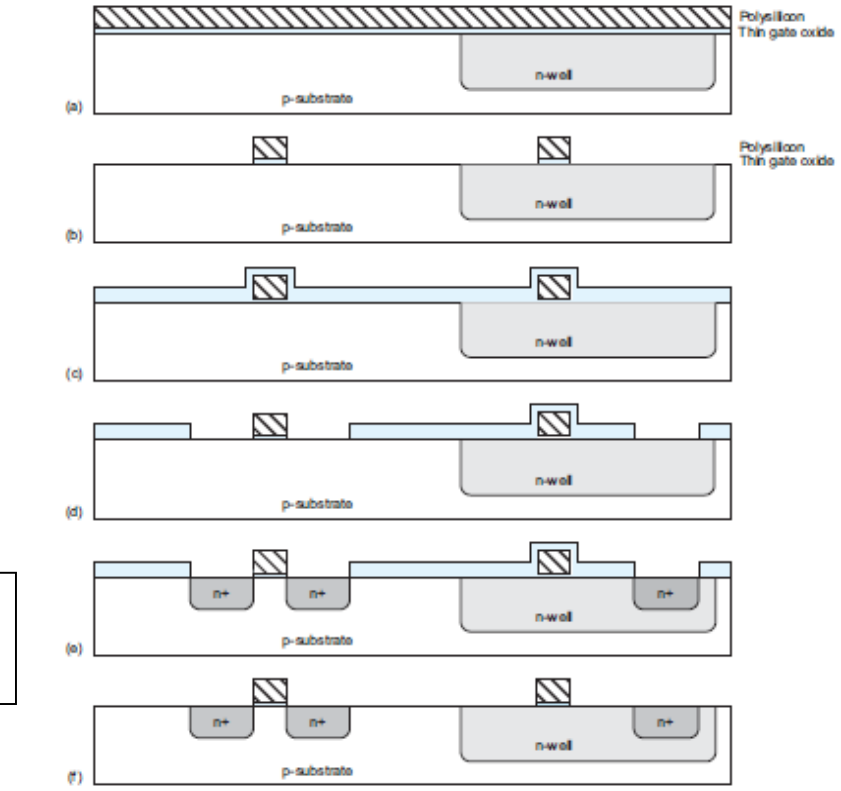
20 transistors.

c.

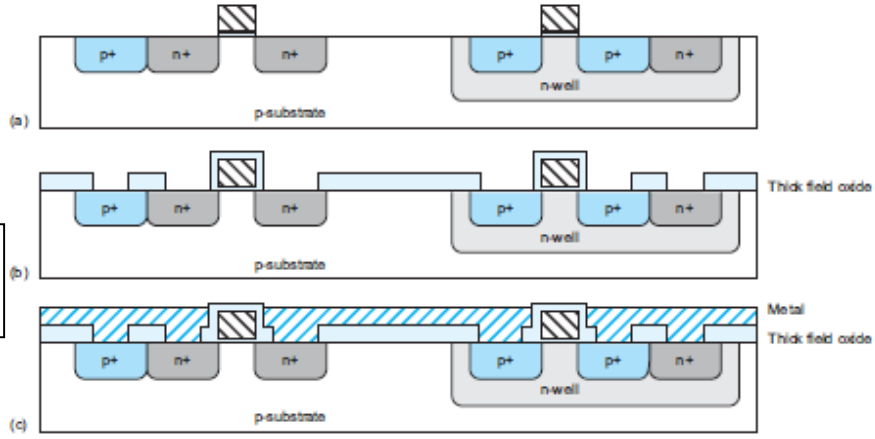
Cross-sections while manufacturing the n-well



Cross-sections while manufacturing polysilicon and n-diffusion

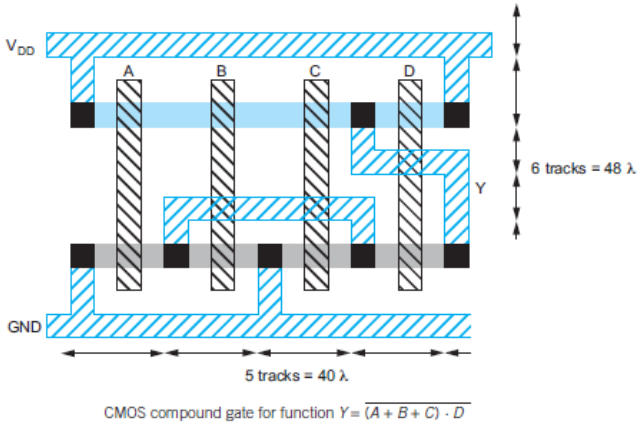


Cross-sections while manufacturing p-diffusion, contacts, and metal



A junction between metal and a lightly doped semiconductor forms a *Schottky diode* that only carries current in one direction. When the semiconductor is doped more heavily, it forms a good ohmic contact with metal that provides low resistance for bidirectional current flow. The substrate must be tied to a low potential to avoid forward-biasing the p-n junction between the p-type substrate and the n+ nMOS source or drain. Likewise, the n-well must be tied to a high potential. This is done by adding heavily doped substrate and well contacts, or *taps*, to connect GND and *VDD* to the substrate and n-well, respectively.

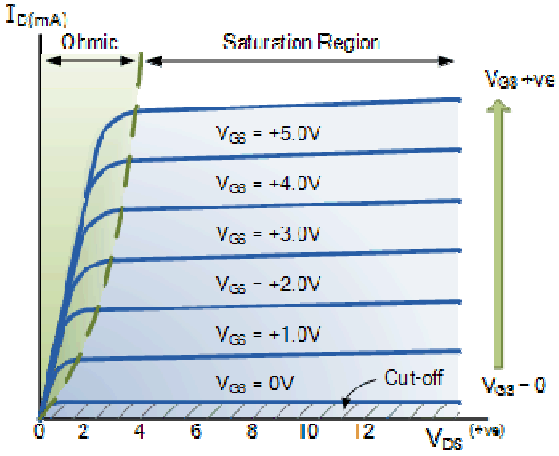
d.



CMOS compound gate for function $Y = \overline{(A + B + C) \cdot D}$

Question (2) **(20 Marks)**

a.



b.

In (a), the transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_{DS}$. The current is

$$I_{DS1} = \frac{\beta}{2}\left(V_{DD} - V_t - \frac{V_{DS}}{2}\right)V_{DS}$$

In (b), the bottom transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_1$. The top transistor sees $V_{gs} = V_{DD} - V_1$ and $V_{ds} = V_{DS} - V_1$. The currents are

$$I_{DS2} = \beta\left(V_{DD} - V_t - \frac{V_1}{2}\right)V_1 = \beta\left((V_{DD} - V_1) - V_t - \frac{(V_{DS} - V_1)}{2}\right)(V_{DS} - V_1)$$

Solving for V_1, we find

$$V_1 = (V_{DD} - V_t) - \sqrt{(V_{DD} - V_t)^2 - \left(V_{DD} - V_t - \frac{V_{DS}}{2}\right)V_{DS}}$$

Substituting V_1 indo the I_{DS2} equation and simplifying gives $I_{DS1} = I_{DS2}$.

The body effect does not change (a) because $V_{sb} = 0$. The body effect raises the threshold of the top transistor in (b) because $V_{sb} > 0$. This lowers the current through the series transistors, so $I_{DS1} > I_{DS2}$.

c.

The new threshold voltage is found as

$$\phi_s = 2(0.026)\ln\frac{2\bullet10^{17}}{1.45\bullet10^{10}} = 0.85V$$

$$\gamma = \frac{100\bullet10^{-8}}{3.9\bullet8.85\bullet10^{-14}}\sqrt{2\left(1.6\bullet10^{-19}\right)\left(11.7\bullet8.85\bullet10^{-14}\right)\left(2\bullet10^{17}\right)} = 0.75V^{1/2}$$

$$V_t = 0.7 + \gamma\left(\sqrt{\phi_s + 4} - \sqrt{\phi_s}\right) = 1.66V$$

d. (a) 0; (b) $2|V_{tp}|$; (c) $|V_{tp}|$; (d) $V_{DD} - V_{tn}$

Question (3) **(15 Marks)**

a.

Velocity saturation.

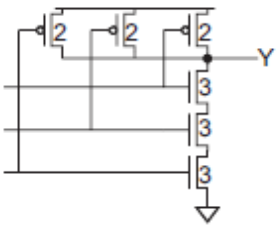
As carriers scattering off the silicon lattice, the faster you try to go, the more often you collide. Beyond a certain level of fatigue, you reach a maximum average speed. In the same way, carriers approach a maximum velocity v_{sat} when high fields are applied

Mobility Degradation.

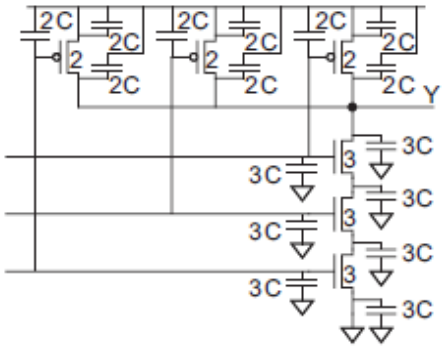
High voltage at the gate of the transistor attracts the carriers to the edge of the channel, causing collisions with the oxide interface that slow the carriers

b. $V_{IL} = 0.3$; $V_{IH} = 1.05$; $V_{OL} = 0.15$; $V_{OH} = 1.2$; $NM_H = 0.15$; $NM_L = 0.15$

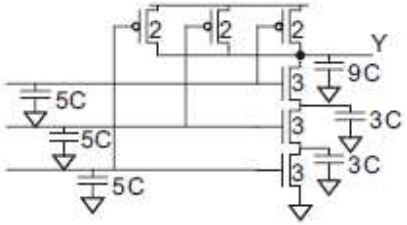
c. Estimate the rising and falling propagation delays (t_{pdr}, t_{pdf}) and the rising and falling contamination delays (t_{cdr} and t_{cdf}) for the 3-input NAND gate if the output is loaded with *h* identical NAND gates using Elmore delay model.

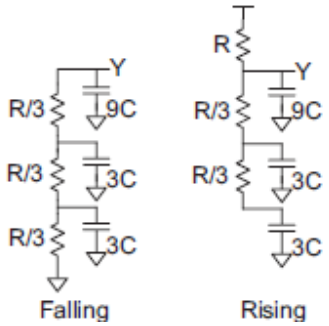


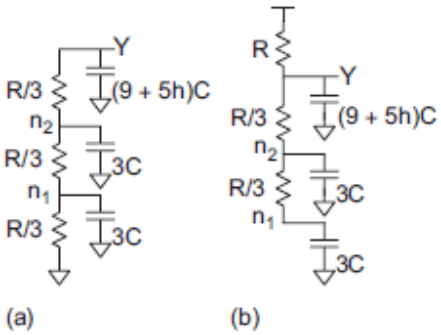
(a)



(b)



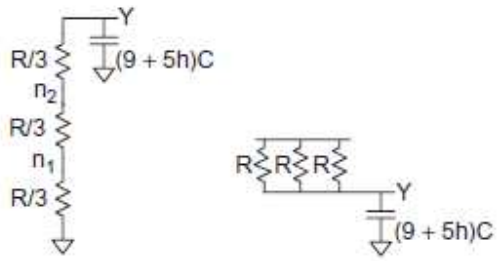




Equivalent circuits for loaded gate

Figure (a) shows the equivalent circuit including the load for the falling transition. Node n_1 has capacitance $3C$ and resistance of $R/3$ to ground. Node n_2 has capacitance $3C$ and resistance $(R/3 + R/3)$ to ground. Node Y has capacitance $(9 + 5h)C$ and resistance $(R/3 + R/3 + R/3)$ to ground. The Elmore delay for the falling output is the sum of these RC products, $t_{pdf} = (3C)(R/3) + (3C)(R/3 + R/3) + ((9 + 5h)C)(R/3 + R/3 + R/3) = (12 + 5h)RC$.

Figure (b) shows the equivalent circuit for the falling transition. In the worst case, the two inner inputs are 1 and the outer input falls. Y is pulled up to V_{DD} through a single pMOS transistor. The ON nMOS transistors contribute parasitic capacitance that slows the transition. Node Y has capacitance $(9 + 5h)C$ and resistance R to the V_{DD} supply. Node n_2 has capacitance $3C$. The relevant resistance is only R, not $(R + R/3)$, because the output is being charged only through R. This is what is meant by the resistance on the shared path from the source (V_{DD}) to the node (n_2) and the leaf (Y). Similarly, node n_1 has capacitance $3C$ and resistance R. Hence, the Elmore delay for the rising output is $t_{pdr} = (15 + 5h)RC$. The $R/3$ resistances do not contribute to this delay. Indeed, they shield the diffusion capacitances, which don't have to charge all the way up before Y rises.



Equivalent circuits
for contamination delay

The contamination delay is the fastest that the gate might switch.

For the falling transition, the best case is that the bottom two nMOS transistors are already ON when the top one turns ON. In such a case, the diffusion capacitances on *n*1 and *n*2 have already been discharged and do not contribute to the delay. Figure (a) shows the equivalent circuit and the delay is

$$t_{cdf} = (9 + 5h)RC.$$

For the rising transition, the best case is that all three pMOS transistors turn on simultaneously. The nMOS transistors turn OFF, so *n*1 and *n*2 are not connected to the output and do not contribute to delay. The parallel transistors deliver three times as much current, as shown in Figure 4.16(b), so the delay is

$$t_{cdr} = (3 + (5/3)h)RC.$$

(Good Luck)