Benha Faculty of Engineering – Benha University		
Spring semester, May 2013		Course: E314 Computer Architecture
Department : Electrical Engineering		Year: 3rd Electronics
Regular Exam	Time: 3 Hrs.	Dr. Mostafa Elsayed

Question #1 **[20 Points]**

(a) [8 points]

A digital computer has a common BUS system for 8 registers of 16-bit each; this bus system allows data transfer between any two registers at a time. For this system do the following:

i. **How many multiplexers are there in the bus?**
ii. **What is the size of each multiplexer?**
iii. **Draw the logic diagram for this BUS system.**

Sol.:

i. Number of multiplexers = 16
ii. Size of each multiplexer = 8 x 1
iii. As in the lecture notes

(b) [12 points]

Consider the basic computer whose instruction set is described by table 1. If the initial content of the AC is 7CE8 and that of PC is D2A and the memory contents are as follow:

Address	D2A	E01	E02
Content	8E01	E02	F436

Show the content of each register (in hexadecimal) to fetch and execute the given instruction by completing the following table:

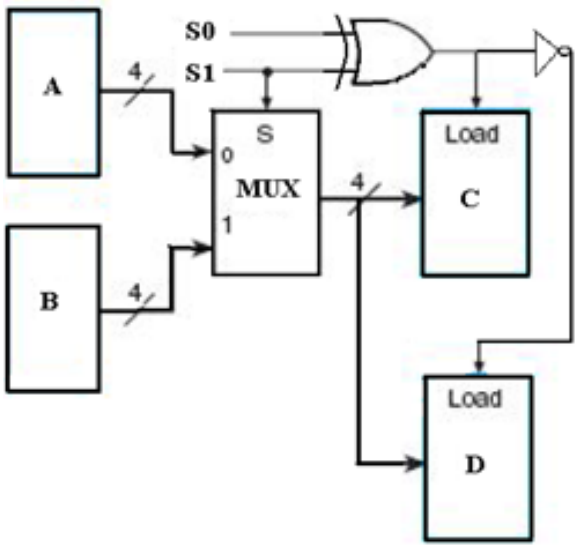
Sol.

Instruction	Phase	Time	Hexadecimal content of the register					
			PC	AC	AR	DR	IR	SC
AND	Fetch	T0	D2A	7CE8	D2A	-	-	0
		T1	D2B	"	"	"	8E01	1
	Decode	T2	"	"	E01	"	"	2
	Address	T3	"	"	E02	"	"	3
	Execute	T4	"	"	"	F436	"	4
		T5	"	7400	"	"	"	5 → 0

Question #2 [18 Points]

(a) (8 points)

For the block diagram shown at the right write its Register Transfer Statement by completing the following table:



Sol.

S1	S0	RTL Statement
0	0	D ← A
0	1	C ← A
1	0	C ← B
1	1	D ← B

(b) Briefly explain the main function of the following special purpose registers:
IR, MAR, MBR, PC, and AC [10 points]

Sol.

1. **IR : Instruction register holds the instruction word to be executed**
2. **MAR : Memory Address Register holds the address of any data from the memory**
3. **MBR : Memory Buffer Register holds any data fetched from the memory**
4. **PC : Program Counter holds the address of the next instruction**
5. **AC : Accumulator general purpose register involved in many arithmetic and logic operations.**

Question #3 **[22 Points]**

a) Consider the basic computer registers connected to a common bus system shown in Fig.(1), for each indicated micro-instruction, complete the following table: [12 points]

Sol.

Microinstruction	Bus select			Source *Register*	Destination Register And controls				Memory	
	S_2	S_1	S_0		*Name*	LD	INR	CLR	Read	Write
AR ← PC	0	1	0	PC	AR	1	0	0	0	0
PC ← PC+1	0	1	0	PC	PC	0	1	0	0	0
IR ← M[AR]	1	1	1	M	IR	1	0	0	1	0
AR ← IR	1	0	1	IR	AR	1	0	0	0	0
DR ←M[AR]	0	1	1	M	DR	1	0	0	1	0
TR ← 0	0	0	0	TR	TR	0	0	1	X	X

b) Consider the basic computer registers connected to a common bus system similar to that shown in Fig.(1), if the memory size is changed to 64K x 24 bits, and the instruction format has three parts: an Indirect address bit (I), the op-code part and the address part for this system perform the following: [10 points]

i. **What is the size of the Op-code and the address fields of the instruction?**
ii. **What is the number of bits of the registers: DR, AR, AC, IR, PC, TR?**

Sol.:

i. Instruction word = 24 bits, address field = 16, so op-code = 24-16-1 = 7-bits

ii. DR = 24, AR = 16, AC= 24, IR = 24, PC = 16, TR = 24.

Good Luck,

Dr. Mostafa Elsayed

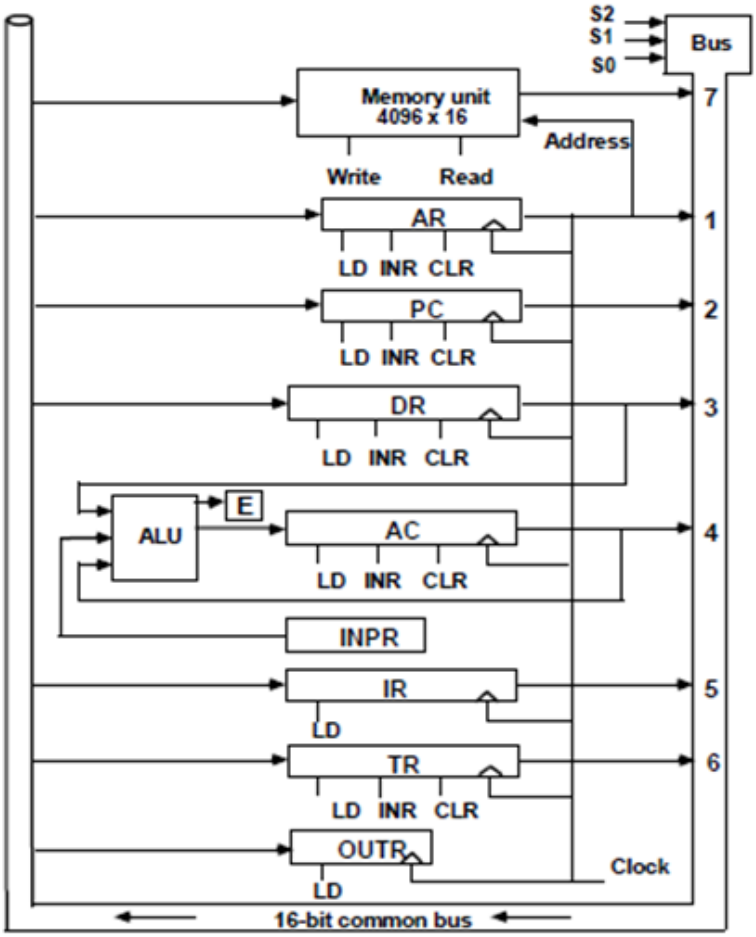


Fig. (1) Basic computer connected to a common bus

Symbol	Hex Code I = 0	Hex Code I = 1	Description
AND	0xxx	8xxx	AND memory word to AC
ADD	1xxx	9xxx	Add memory word to AC
LDA	2xxx	Axxx	Load AC from memory
STA	3xxx	Bxxx	Store content of AC into memory
BUN	4xxx	Cxxx	Branch unconditionally
BSA	5xxx	Dxxx	Branch and save return address
ISZ	6xxx	Exxx	Increment and skip if zero
CLA	7800		Clear AC
CLE	7400		Clear E
CMA	7200		Complement AC
CME	7100		Complement E
CIR	7080		Circulate right AC and E
CIL	7040		Circulate left AC and E
INC	7020		Increment AC
SPA	7010		Skip next instr. if AC is positive
SNA	7008		Skip next instr. if AC is negative
SZA	7004		Skip next instr. if AC is zero
SZE	7002		Skip next instr. if E is zero
HLT	7001		Halt computer
INP	F800		Input character to AC
OUT	F400		Output character from AC
SKI	F200		Skip on input flag
SKO	F100		Skip on output flag
ION	F080		Interrupt on
IOF	F040		Interrupt off

Table 1 instruction set of given architecture