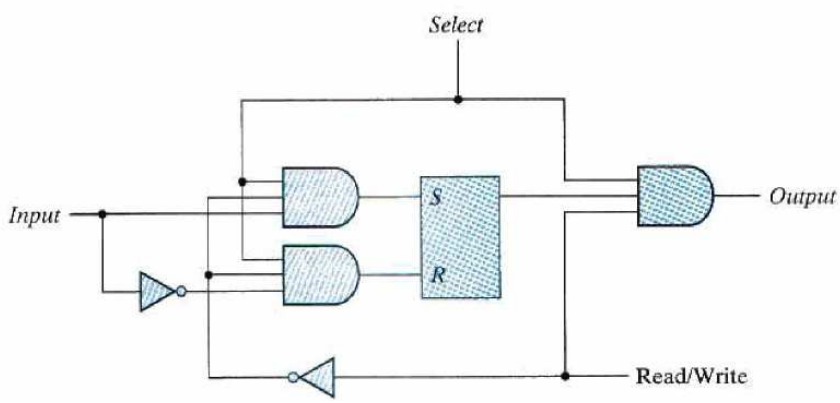
**Benha Faculty of Engineering** | **Electrical Engineering Department**
**3rd Year Electronics** | **Final Exam: 31 December 2014**
**Examiner: Dr. Hatem ZAKARIA** | **Time allowed: 3 Hours**

# Digital Logic Circuits Analysis (E321)

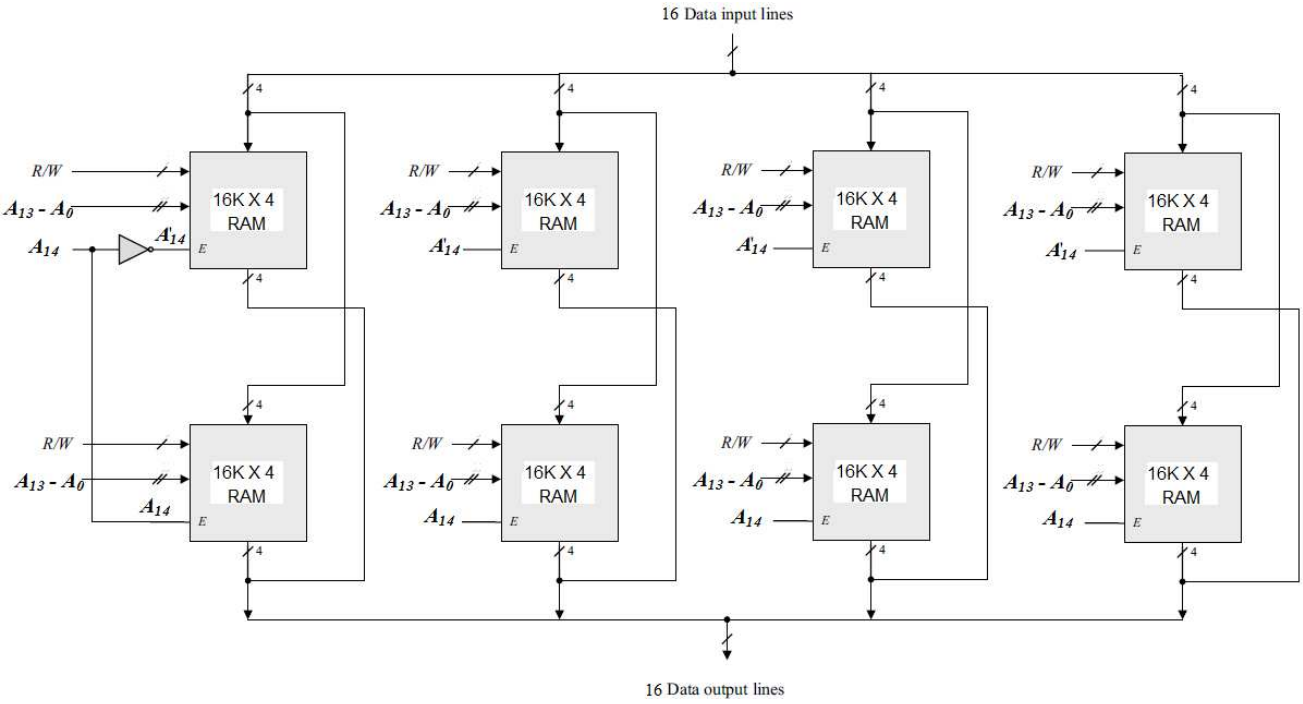
**Model Answer** | **No. of Questions: 5**

**Question (1)** **(12 Marks)**

a. Draw the equivalent logic diagram of a binary cell "basic building block of a RAM" that stores one bit of information. ***(3 Marks)***




b. Given a 16K X 4 RAM chip with an enable input, show the external connections necessary to construct a 32K X 16 RAM with the 16K X 4 RAM chips and a decoder. ***(5 Marks)***



c. Given the 8-bit data word 01011011, generate the 13-bit composite word for the Hamming code that corrects single errors and detect double errors. ***(4 Marks)***

| 01011011 = | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $P_1$ | $P_2$ | 0 | $P_4$ | 1 | 0 | 1 | $P_8$ | 1 | 0 | 1 | 1 | $P_{13}$ |

$P_1$ = Xor of bits (3, 5, 7, 9, 11) = 0, 1, 1, 1, 1 = 0 (Note: even # of 0s)
$P_2$ = Xor of bits (3, 6, 7, 10, 11) = 0, 0, 1, 0, 1 = 0
$P_4$ = Xor of bits (5, 6, 7, 12) = 1, 0, 1, 1 = 1 (Note: odd # of 0s)
$P_8$= Xor of bits (9, 10, 11, 12) = 1, 0, 1, 1, = 1

Composite 13-bit code word: 0001 1011 1011 1

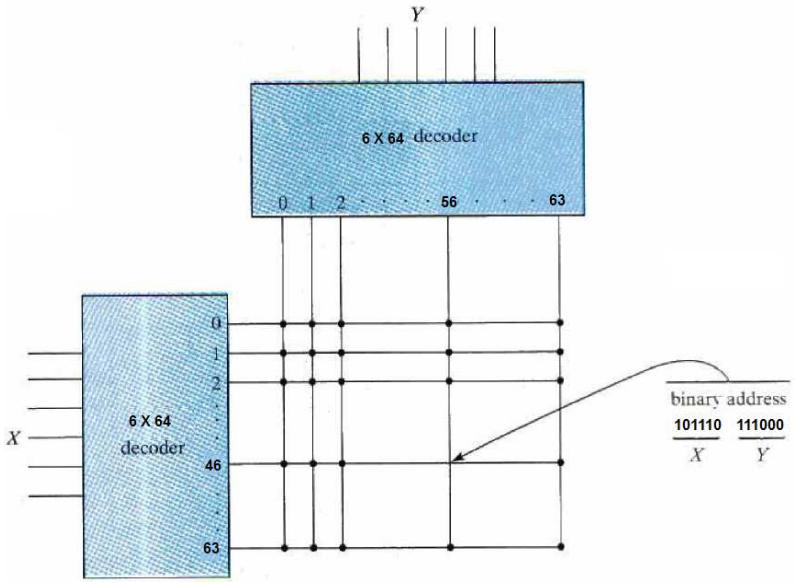
**Question (2)** **(11 Marks)**

a. A 4K X 8 memory uses coincident decoding by splitting the internal decoder into *X*-selection and *Y*-selection.

1. What is the size of each decoder, and how many AND gates are required for decoding the address? What's the number of inputs per each AND gate? ***(3 Marks)***

$4\ K = 2^{12} = 2^6 \times 2^6 = 64 \times 64$
Each decoder is 6 X 64
Decoders require 128 AND gates, each with 6 inputs

2. Draw the structure of such two dimensional decoding? Determine the *X* and *Y* selection lines that are enabled when the input address is the binary equivalent 3000. ***(3 Marks)***

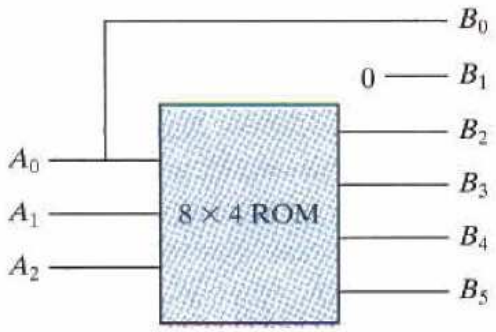



3,000 = 101110_111000
$x$ = 46 and $y$ = 56

b. Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number. Showing the ROM implementation (i.e. its size and connections with external inputs and outputs) and tabulate its truth table. ***(5 Marks)***

*Truth Table for Circuit*

| Inputs | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | Decimal |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 16 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 25 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 36 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 49 |




(a) Block diagram

| $A_2$ | $A_1$ | $A_0$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |

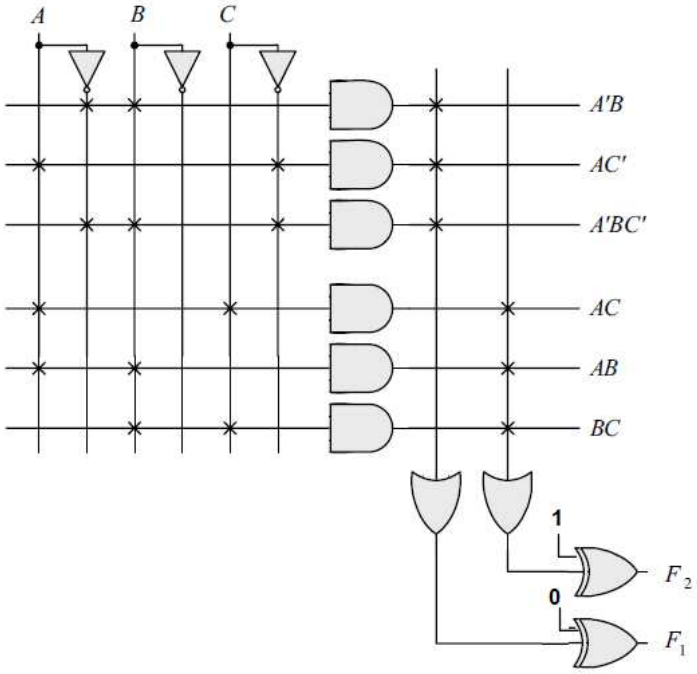
(b) ROM truth table

**<u>Question (3)</u>** **(10 Marks)**

a. Draw a PLA circuit to implement the functions ***(4 Marks)***

$$F_1 = A'B + AC' + A'BC'$$

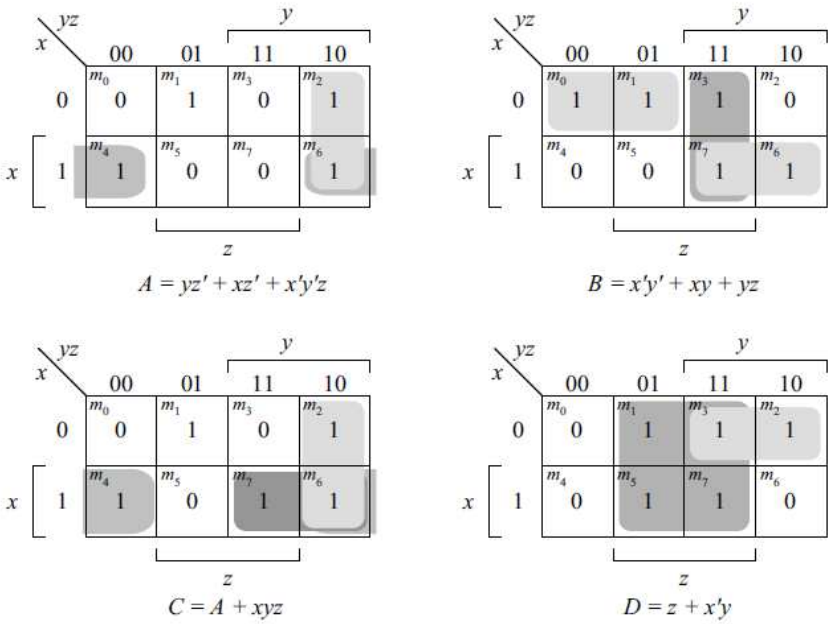
$$F_2 = (AC + AB + BC)'$$



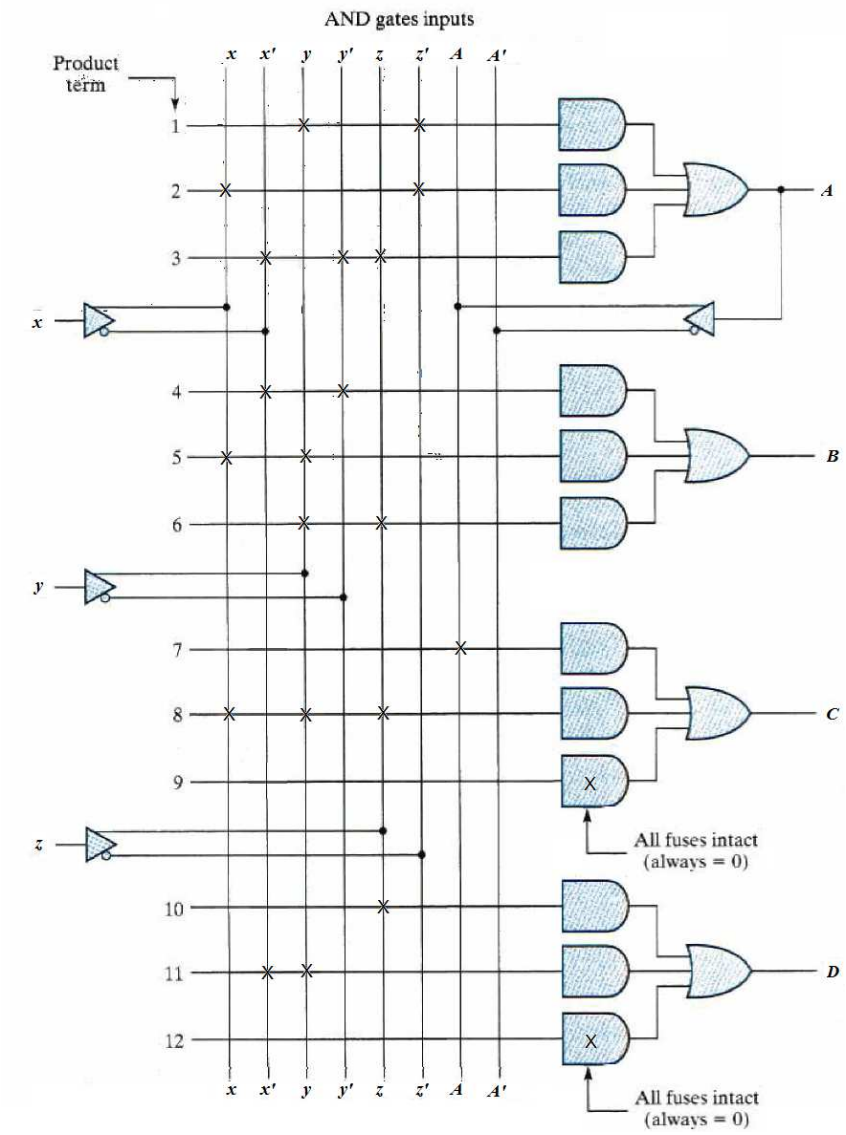

b. The following is a truth table of a three-input, four-output combinational circuit:

$$A(x, y, z) = \sum (1, 2, 4, 6)$$
$$B(x, y, z) = \sum (0, 1, 3, 6, 7)$$
$$C(x, y, z) = \sum (1, 2, 4, 6, 7)$$
$$D(x, y, z) = \sum (1, 2, 3, 5, 7)$$

Tabulate the PAL programming table for the circuit, and mark its fuse map diagram. ***(6 Marks)***

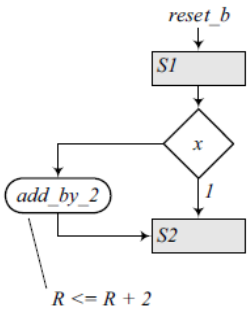


| Product term | AND Inputs x y z A | Outputs |
|---|---|---|
| 1 | - 1 0 - | A = yz' + xz' + x'y'z |
| 2 | 1 - 0 - | |
| 3 | 0 0 1 - | |
| 4 | 0 0 - - | B = x'y' + xy + yz |
| 5 | 1 1 - - | |
| 6 | - 1 1 - | |
| 7 | - - - 1 | C = A + xyz |
| 8 | 1 1 1 - | |
| 9 | - - - - | |
| 10 | - - 1 - | D = z + x'y |
| 11 | 0 1 - - | |
| 12 | - - - - | |



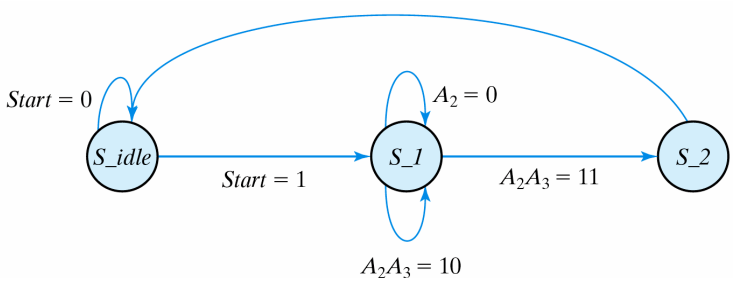
**Question (4)** **(12 Marks)**

a. Draw the ASMD charts for the following state transition:
   - If $x = 1$, control goes from state S1 to state S2; if $x = 0$, generate a conditional operation to increment R by 2 and go from S1 to S2. ***(6 Marks)***

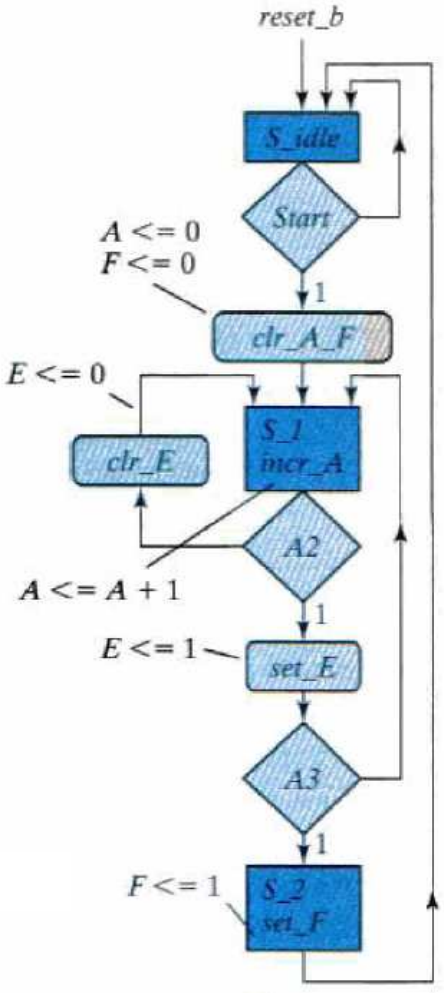



b. The state diagram and the register transfer level description of a control unit are shown below. It has 3 states and 3 inputs (Start, A2 and A3)

S_idle ⟶ S_1, clr_A_F:
S_1 ⟶ S_1, incr_A:
if ($A_2 = 1$) then set_E
if ($A_2 = 0$) then clr_E
S_2 ⟶ S_idle, set_F:



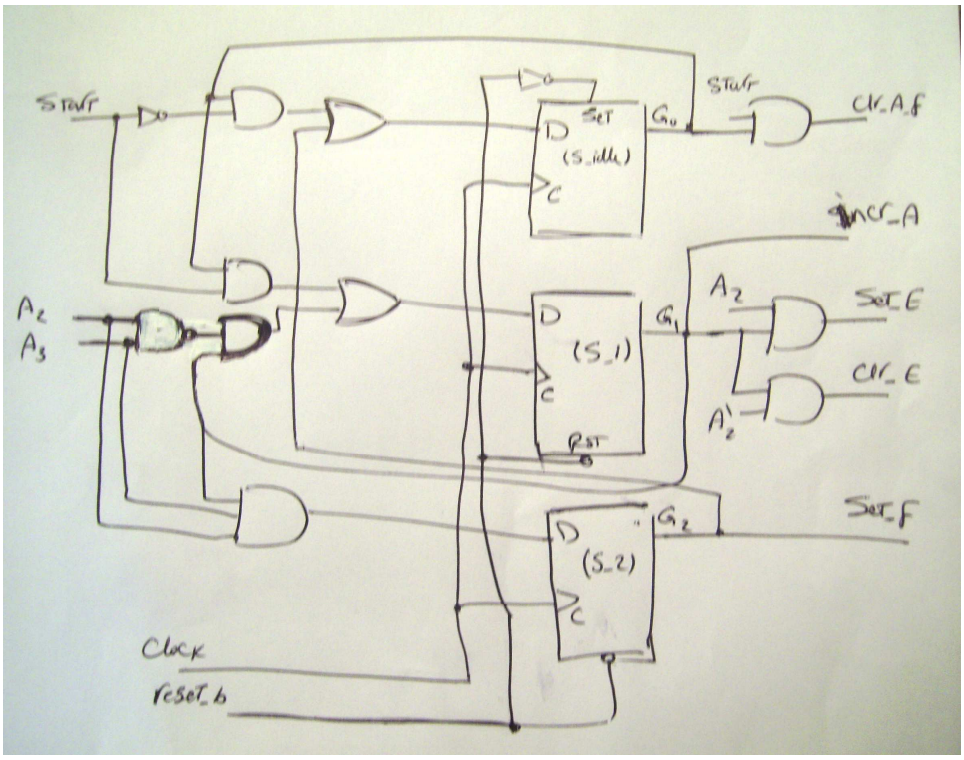

1. Draw the equivalent ASMD chart. ***(3 Marks)***



2. Design the control circuit with one *D* flip flop per state. ***(2 Marks)***

Design equations:

$D_{S\_idle}$ = S_2 + S_idle Start'
$D_{S\_1}$ = S_idle Start + S_1 ($A_2$ $A_3$)'
$D_{S\_2}$ = $A_2$ $A_3$ S_1




3. Design the control unit with *D* flip flops, a decoder, and gates. ***(2 Marks)***

*State Table for the Controller*

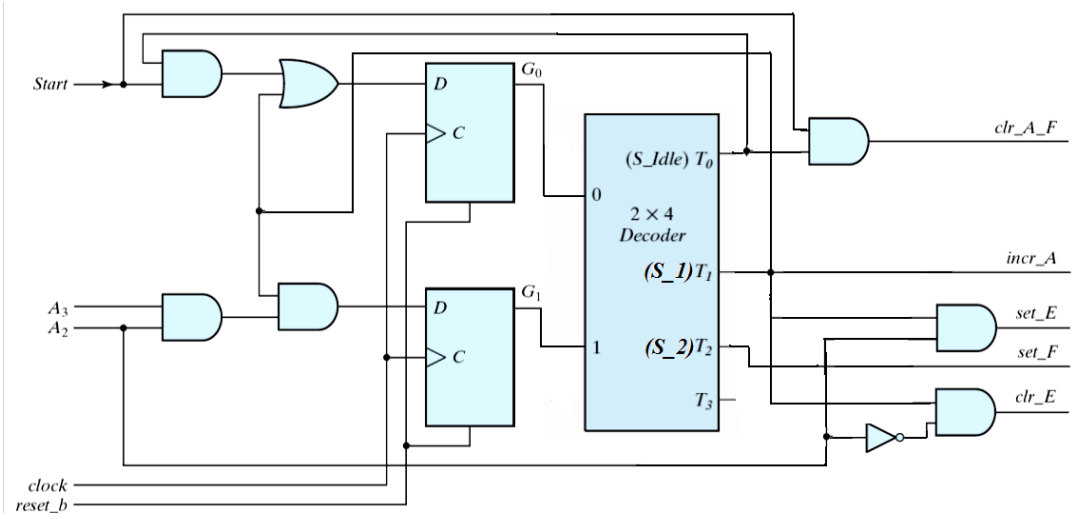
| Present-State Symbol | Present State $G_1$ | Present State $G_0$ | Inputs *Start* | Inputs $A_2$ | Inputs $A_3$ | Next State $G_1$ | Next State $G_0$ | Outputs *set_E* | Outputs *clr_E* | Outputs *set_F* | Outputs *clr_A_F* | Outputs *incr_A* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *S_idle* | 0 | 0 | 0 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| *S_idle* | 0 | 0 | 1 | X | X | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| *S_1* | 0 | 1 | X | 0 | X | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| *S_1* | 0 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| *S_1* | 0 | 1 | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| *S_2* | 1 | 1 | X | X | X | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

$DG_0 = Start\ S\_idle + S\_1$

$DG_1 = S\_1\ A2\ A3$

$set\_E = S\_1\ A2$ $clr\_E = S\_1\ A2'$

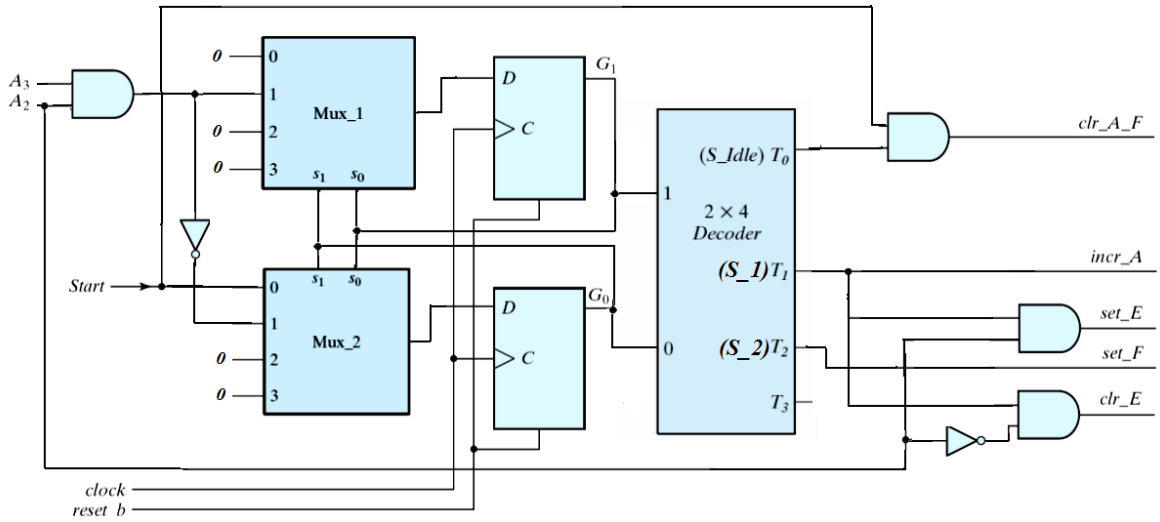
$set\_F = S\_2$ $clr\_A\_F = Start\ S\_idle$ $incr\_A = S\_1$




4. Design the control unit with multiplexers, a register, and a decoder. ***(2 Marks)***

***Multiplexer Input Conditions***

| Present State | | Next State | | Input Condition | Inputs | |
|---|---|---|---|---|---|---|
| $G_1$ | $G_0$ | $G_1$ | $G_0$ | $s$ | MUX1 | MUX2 |
| 0 | 0 | 0 | 0 | $start'$ | 0 | $start$ |
| 0 | 0 | 0 | 1 | $start$ | | |
| 0 | 1 | 0 | 1 | $A_2'$ | | |
| 0 | 1 | 0 | 1 | $A_2A_3'$ | $A_2A_3$ | $(A_2A_3)'$ |
| 0 | 1 | 1 | 0 | $A_2A_3$ | | |
| 1 | 0 | 0 | 0 | *None* | 0 | 0 |



**Question (5)** **(12 Marks)**

a. Explain the difference between asynchronous and synchronous sequential circuits. ***(2 Marks)***

Asynchronous circutis do not use clock pulses and change state in response to input changes.
Synchronous circuits use clock pulses and a change of state occurs in reponse to the clock transition.

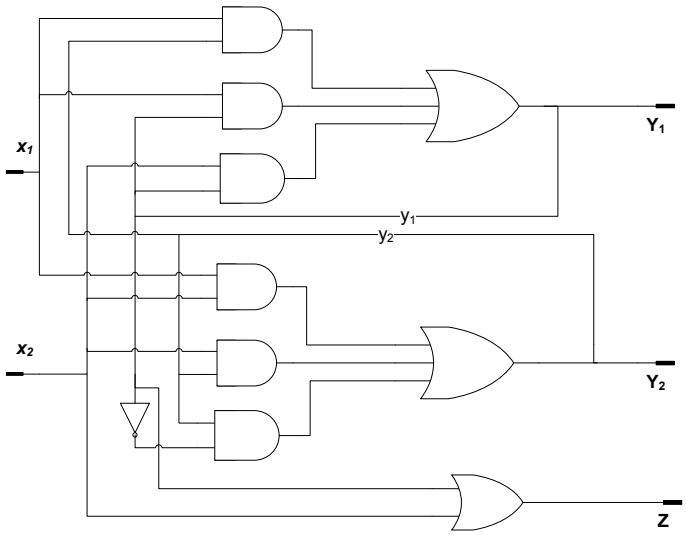
b. Define the fundamental-mode operation. ***(1 Marks)***

The input signals change one at a time when the circuit is stable

c. An asynchronous sequential circuit has two internal states and one output The two excitation functions and one output function describing the circuit are, respectively,

$$Y_1 = x_1y_2 + x_1y_1 + x_2y_1$$
$$Y_2 = x_1x_2 + x_2y_2 + y_1'y_2$$
$$z = x_2 + y_1$$

1. Draw the logic diagram of the circuit. ***(1 Marks)***




2. Derive the transition table and output map. ***(2 Marks)***

| $y_1y_2$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | (00) | (00) | 01 | (00) |
| 01 | (01) | (01) | 11 | 11 |
| 11 | 00 | (11) | (11) | 10 |
| 10 | 00 | (10) | 11 | (10) |

**Transition Table**

| $y_1y_2$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 1 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

**Output Map**

3. Determine all race conditions and whether they are critical or noncritical. ***(2 Marks)***

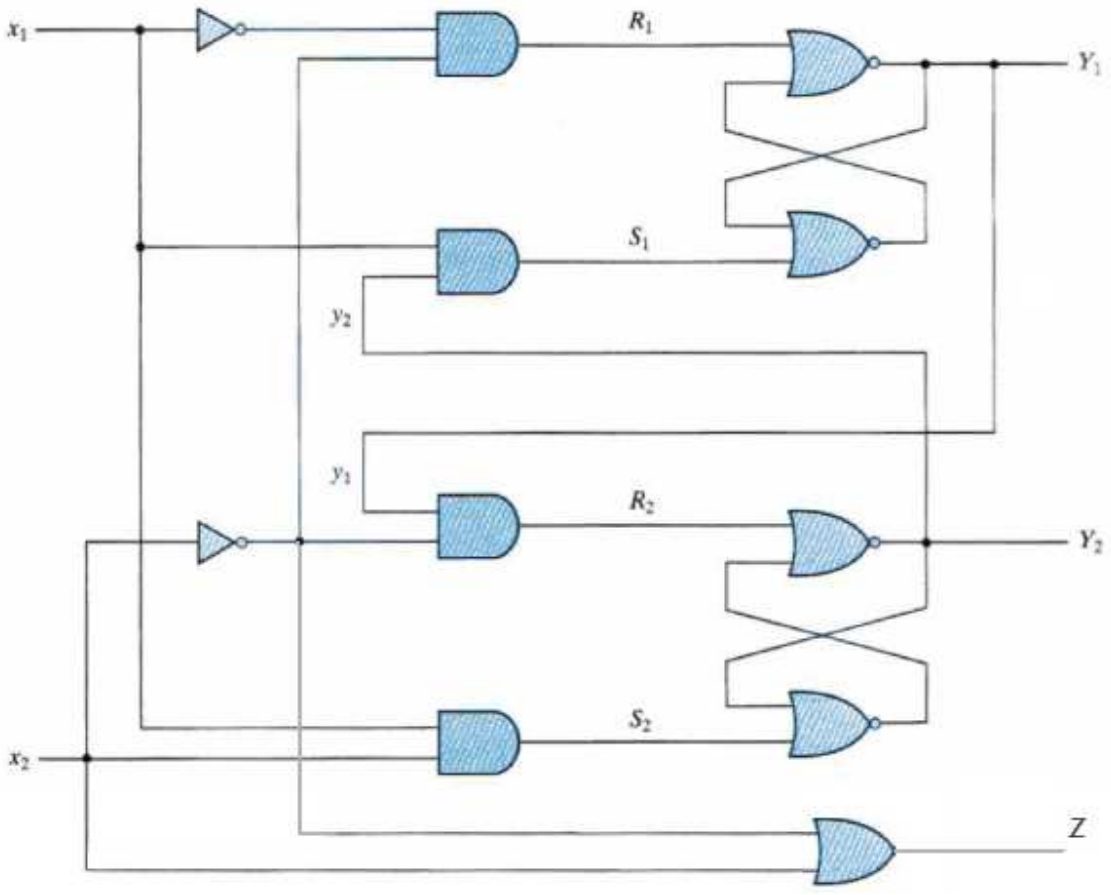
Investigating the transition table, we deduce that the circuit is stable. There is a critical race condition when the circuit is initially in total state $y_1y_2x_1x_2$= 1 10 1 ($Y_1Y_2$ = 1 1) and $x_2$ changes from 1 to 0 ($Y_1Y_2$= 00). If $Y_1$ changes to 0 before $Y_2$, the circuit goes to total state 0100 instead of 0000.

4. Implement the circuit with NOR *SR* latches. ***(4 Marks)***

$$S_1 = x_1y_2 \qquad S_2 = x_1x_2$$
$$R_1 = x_1'x_2' \qquad R_2 = x_2'y_1$$

We then check whether the condition $SR = 0$ is satisfied to ensure proper operation of the circuit:

$$S_1R_1 = x_1y_2x_1'x_2' = 0$$
$$S_2R_2 = x_1x_2x_2'y_1 = 0$$




**(Good Luck)**